29.5 A 200mA 93% Peak Efficiency Single-Inductor Dual-Output DC-DC Buck Converter

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The fast market growth of battery-operated portable applications such as digital cameras, personal digital assistants, cellular phones, MP3 players, medical diagnosis systems, and so on demands more and more efficient power management systems. In this area, DC-DC converters play a critical role in keeping long battery life while still providing stable supply voltages together with the required driving capability [1]. Key features of DC-DC converters are high power efficiency, low cost, and small size.

Recently, in portable applications, a widely adopted strategy to reduce power consumption consists of using multiple supply voltages for different functional blocks [2]. In a number of applications, the need for multiple supply voltages lower than the battery voltage is common. In these cases, conventional implementations of DC-DC buck converters [3,4] typically consist of N independent converters, where N is the number of required output voltages. This solution wastes components and, hence, area. Furthermore, this method increases the cost of the system. The need for devices capable of supplying independent loads by minimizing the number of external components is, therefore, evident.

This single-inductor dual output (SIDO) DC-DC buck converter uses only one (external) inductor to provide two independent output voltages ranging from 1.2V to the power supply (2.6 to 5V), achieving a peak efficiency of 93.3% with a maximum total output current of 200mA.

The basic idea of this DC-DC buck converter is to share the magnetic energy stored in the single inductor in order to supply two different and independent loads. By using a dedicated control strategy, the current flowing through the inductor can be switched from one load to the other, according to the needs of the loads.

Figure 29.5.1 shows the circuit diagram of the proposed single-inductor dual output DC-DC buck converter. The inductor L is connected to the output branches by means of the p-type MOS transistors M_2 and M_3. The bulk terminals of transistors M_2 and M_3 are dynamically biased to the higher voltage between *IND+* and the output voltages by means of blocks *BB1* and *BB2*, respectively. Storage capacitors C_1 and C_2 act as filters for the two output voltages, V_{OUT1} and V_{OUT2}, respectively, while R_1 and R_2 represent the corresponding output loads. To correctly manage the system, two feedback-control loops are required, whose complexities critically depend on the desired ripple for each output. For circuits that allow 50mV ripple, the best trade-off consists of using two PWM pulses controlled by the error amplifiers A_1 and A_2 that, together with the comparators CMP_1 and CMP_2 and the triangular shaped waveform generator *TRIANG GEN*, produce the signals D_1 and D_2. Transistor M_1, driven by PWM signal D_1, controls the amount of input power to be injected into the DC-DC converter. Transistor M_4 connects the inductor to ground when M_1 is turned-off. Transistors M_2 and M_3, controlled by PWM signals D_2 and $D_{2,n}$ respectively, distribute the input power to the loads, according to the required currents.

PMOS transistors M_1, M_2, and M_3 have W/L ratios of 18000/0.6, while NMOS transistor M_4 is 6000/0.6. Component sizes for transistors M_j (j = 1, …,4) are determined based on a trade-off between the on-resistance of the switches and the silicon area together with the dynamic power consumption. To be more specific, the higher the transistor width, the lower will be the on-resistance and, hence, the higher the overall power efficiency of the system. It has to be pointed out that the transistor width has an upper bound due to the dynamic power consumption. The minimum channel length has not been adopted in order to minimize transistor leakage currents.

Figure 29.5.2 shows the circuit diagram of blocks *BB1* and *BB2* represented in Fig. 29.5.1. Block *BB1* dynamically biases the bulk terminal of M_2 to the higher voltage between *IND+* and V_{OUT1}. By means of block *BB2*, the higher voltage between *IND+* and V_{OUT2} biases the bulk terminal of M_3. This results in a reduction of the body effect contribution on these transistors and, hence, in a lower on-resistance and a higher power efficiency.

The proposed converter has been fabricated in a 0.35µm p-substrate CMOS technology. Figure 29.5.3 depicts the measured output voltages. The power supply is equal to 3.6V. V_{OUT1} and V_{OUT2} are set to 3.3 and 1.8V, respectively. The measured voltage ripple is 31mV for V_{OUT1} and 24mV for V_{OUT2}, when the output currents are equal to 56 and 40mA, respectively.

Figure 29.5.4 shows the cross coupling between the output voltages with one output fixed at 3.3V (V_{OUT1}) and the other (V_{OUT2}) changing by 680mV, from 1.42 to 2.1V. Notice that the increase in the current on the second load from 22 to 33mA does not affect V_{OUT1} at all.

Figure 29.5.5 shows the measured power efficiency of the system. By keeping the power supply set to 3.6V and the output current on the second load equal to 40.2mA, the power efficiency, measured as a function of the first output current, reaches 93.3% when both output voltages are set to 3.3V and the overall output current is 124.8mA. When the output voltages are set to 3.3 and 1.8V, the power efficiency reaches 85.2% when the overall output current is 190mA. The power efficiency is always higher than 62.5%. The high measured power efficiency also depends on the automatic substrate bias switch that cancels the body bias effect of the p-channel transistors M_2 and M_3. Figures 29.5.6 and 29.5.7 show the performance summary and the chip micrograph, respectively.

References:

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[4] V. Kursun, S. G. Narenda, V. K. De and E. G. Friedman, "Analysis of Buck Converters for On-Chip Integration with a Dual Supply Voltage Microprocessor," *IEEE T. VLSI Systems* vol. 11, pp. 514-522, June, 2003.

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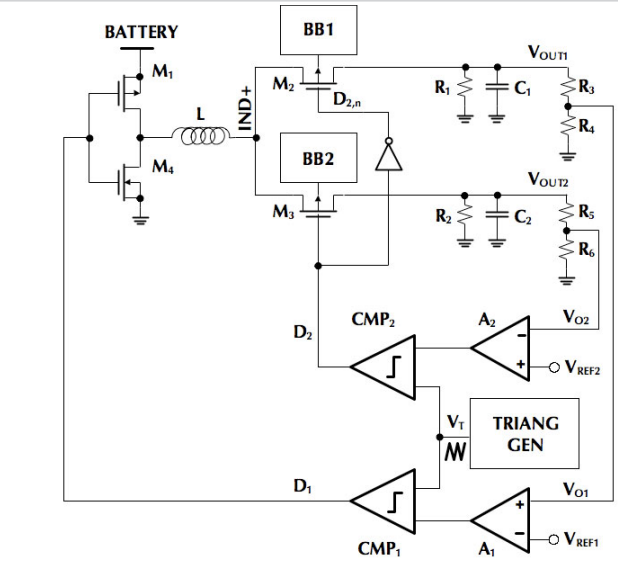

Figure 29.5.1: SIDO buck converter circuit.

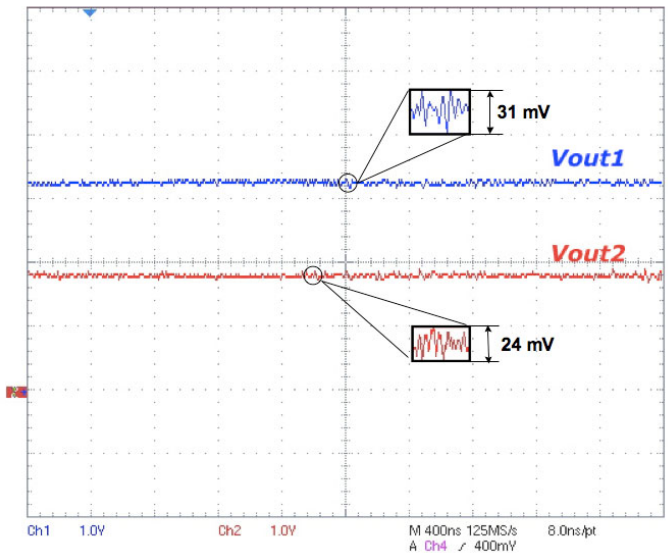

Figure 29.5.3: Measured output voltages.

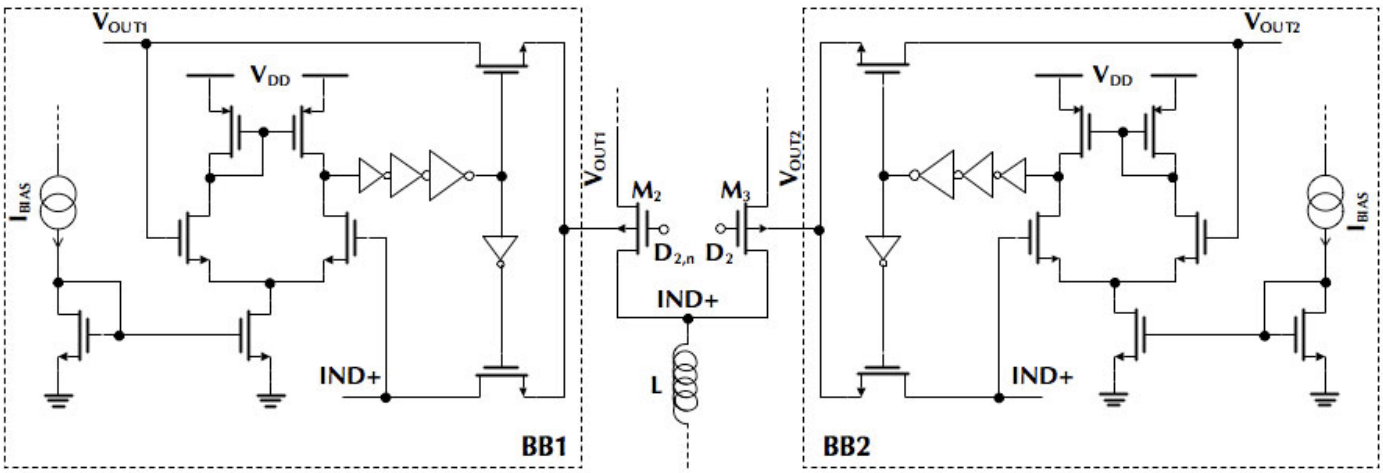

Figure 29.5.2: Bulk-bias circuit schematic.

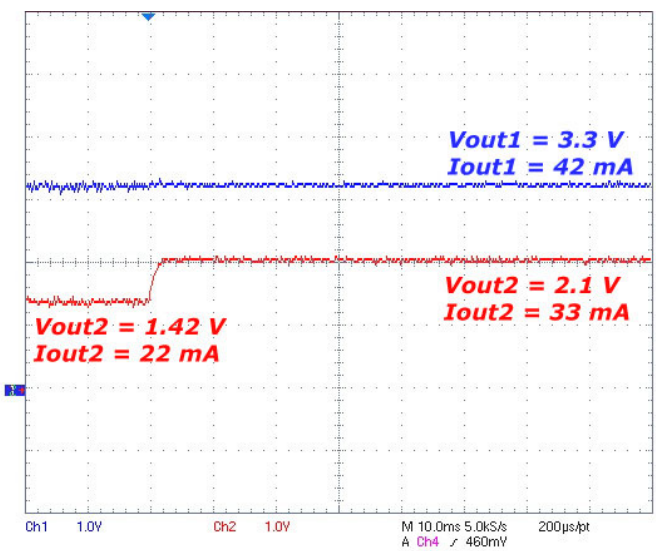

Figure 29.5.4: Measured step response.

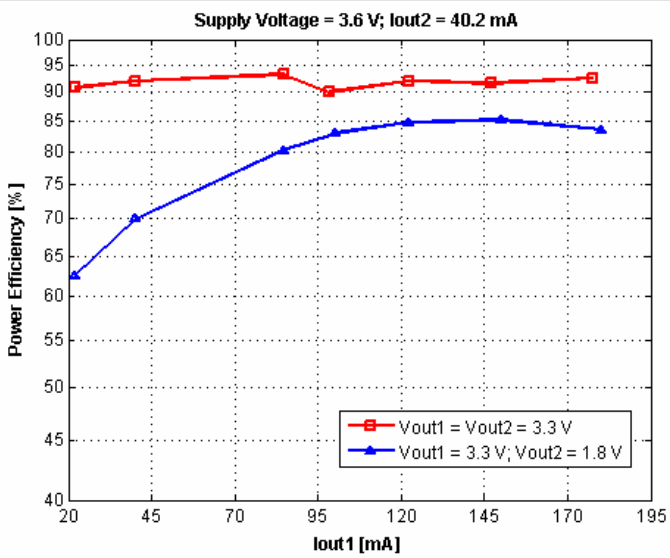

Figure 29.5.5: Measured power efficiency.

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Supply voltage range (V_{in})	2.6V - 5V
Regulated output voltages	1.2V - V_{in} 1.2V - V_{in}
Switching frequency	1MHz
Output capacitors (off-chip)	35µF
Inductor (off-chip)	22µH
Overall output current range	0 - 200mA
Maximum power efficiency	93.3%
Technology	0.35-µm p-substrate (3-metal, 1-poly)
Chip area	1350µm × 1800µm (including pads)

Figure 29.5.6: Performance summary.

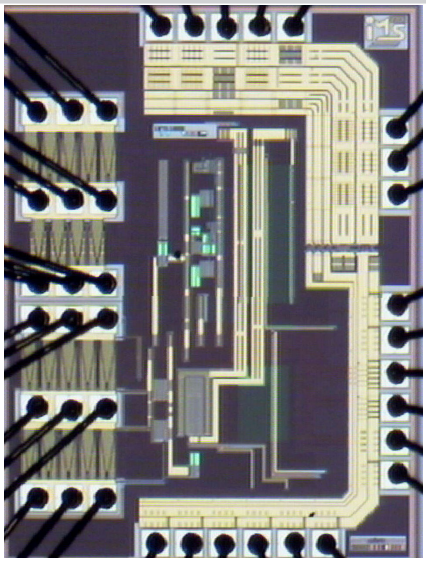

Figure 29.5.7: SIDO buck converter chip micrograph.

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